DOCKET NO. 02-IND-369 PATENT

CONTENT ADDRESSABLE MEMORY ARCHITECTURE PROVIDING IMPROVED SPEED

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CONTENT ADDRESSABLE MEMORY ARCHITECTURE PROVIDING IMPROVED SPEED

TECHNICAL FIELD OF THE INVENTION

[0001] The invention relates generally to the field of binary Content Addressable Memory ("CAM") applications. More particularly the invention relates to a method and device providing improved performance by utilizing both phases of the clock cycles.

BACKGROUND OF THE INVENTION

[0002] A content addressable memory CAM architecture is an array of individual CAM cells. Each CAM cell consists of a data storage unit and comparison circuitry. The storage unit is used for storing data and the comparison circuitry is used to compare the compare-data with the data stored in storage unit and providing a signal indicating a match or mismatch. This signal is fed to a priority encoder for selecting one of the match signal, in the vent of multiple as the final output.

[0003] Throughout this disclosure, logical "1" refers to and is interchangeable with a logical "High" corresponding to a voltage VDD, while logical "0" refers to and is interchangeable with a logical "Low" corresponding to GND. Figure 1 illustrates a PRIOR ART 9-

transistor CAM cell 100 using a NOR configuration. The CAM cell 100 includes an SRAM cell for data storage, comprising a pair of cross-coupled inverters formed by transistors 111, 112, 113 and 114 and a pair of access transistors 115 and 116. The comparison circuitry of the CAM cell 100 consists of a pair of pass transistors 117 and 118. The conducting terminals of the pass transistor 113 and 111 are connected in series between the supply voltage VDD and ground GND while the control terminals are connected to the common conducting terminals F of pass transistors 114 and 112. The conducting terminals of pass transistor 114 and 112 are also connected in series between VDD and GND while the control terminals are connected to the common conducting terminals T of pass transistors 113 and 111. The conducting terminals of pass transistors 115 and 116 connect nodes T and F to the corresponding bit lines BLT and BLF while the control terminals are connected to word line WL. The pass transistors 117 and 118 are connected in series between bit lines BLT and BLF and the common node is labeled as the Bit-Match node. The control terminals of transistors 117 and 118 are coupled to nodes F and T, respectively. Output transistor 119 is coupled between the match line ML and ground GND and its control terminal is connected to the Bit-Match node of the CAM cell.

[0004] The READ and WRITE operations of this CAM cell 100 are the same as those of a standard 6-transistor SRAM cell, wherein the precharge state of bit lines BLT and BLF is logical "High". During the SEARCH operation, bit lines BLT and BLF are initially precharged to logical "Low" and ML is precharged to logical "High". Then the comparand bit is placed on BLT and its complement is placed on BLF. If the comparand bit matches with the data bit stored in the CAM cell, then one of the pass transistors 117 or 118 drives the Bit-Match node to logical "0" and therefore ML remains at logical "High", indicating a match. On the other hand, if there is a mismatch between the applied comparand bit and the data bit stored in the CAM cell, then one of the pass transistors 117 or 118 drives the Bit-Match node to "VDD-Vtn", thereby turning the pull-down transistor 119 on and pulling down ML indicating a mismatch.

[0005] The CAM cell 100 requires a precharge to logical "Low" operation for bit lines and a precharge to logical "High" operation for ML when a SEARCH operation is requested if the default standby state is for a READ or a WRITE operation. Conversely, if the CAM cell 100 is ready for a SEARCH operation in its default standby state, then the bit lines must be precharged to logical "High" and ML is thereby discharged when a READ or WRITE operation is requested. It is known that both bit lines

and ML impose a heavy capacitive load on their drivers and prechargers. Therefore, CAM cell 100 consumes more power and provides larger READ/WRITE/ SEARCH access times.

[0006] Figure 2 illustrates another PRIOR ART 9-transistor CAM cell 200 using a NOR configuration. The only difference between CAM cell 100 and 200 is that CAM cell 200 is provided with dedicated lines CBLT and CBLF for the search operation as shown in the figure 2. Thus, CAM cell 200 provides more flexibility in the timing of READ, WRITE and SEARCH operations but at the cost of hardware overhead required for controlling the dedicated compare bit lines CBLT and CBLF.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, a primary object of the present invention is to obviate the above drawbacks and provide memory architecture with higher speed and smaller size.Another object of the invention is to combine "compare and write" or "compare and read" operations in one clock cycle to increase the speed of operation without increasing the area of the chip.

[0008] To achieve the objectives, this invention provides a Content Addressable Memory (CAM) architecture providing improved speed, comprising:

- an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively,
- outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and;
- a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within

the second state of the same clock cycle in the event of a match.

[0009] The control logic comprising a sequencing circuit that enables the data comparators of the CAM cell array and the address decoder of read/write block during the first state of the clock and enables the read-or-write operation in the second state of the same clock.

[00010] The invention further provides a method for improving speed of a Content Addressable Memory (CAM) architecture comprising the steps of:

- connecting an array of CAM cells to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and writing data in the CAM cell respectively,
- coupling a match block to said array of CAM cell providing match outputs signal lines for identifying a match/no-match at the end of a Search operation,
- performing the search and address decoding operations during first state of the clock cycle, and;
- implementing the read/write operation after a successful search during the second state of the same clock cycle.

[00011] Before undertaking the DETAILED DESCRIPTION OF THE INVENTION below, it may be advantageous to set

forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; and the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior, as well as future uses of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[00012] The present invention will now be described with reference to the accompanying drawings, in which like reference numerals represent like parts, and in which:

Figure 1 shows a PRIOR ART 9-transistor CAM cell architecture;

Figure 2 shows another PRIOR ART 9-transistor CAM cell architecture;

Figure 3 shows a block diagram of an exemplary CAM architecture in accordance with the present invention;

Figure 4 shows a data flow chart of a decoder;

Figure 5 shows a data flow chart for the normal read and write operation;

Figure 6 shows a timing diagram for the normal read operation;

Figure 7 shows a timing diagram for the normal write operation;

Figure 8 shows a timing diagram for the normal compare operation;

Figure 9 shows a timing diagram for the combine operation of compare and read; and

Figure 10 shows a timing diagram for the combine operation of compare and write.

DETAILED DESCRIPTION OF THEINVENTION

[00013] Figures 1 and 2 have already been described with reference to PRIOR ART implementations under the background to the invention. Figures 3 through 10, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any suitably arranged Content Addressable Memory ("CAM") architecture.

[00014] Figure 3 shows a block diagram of a CAM memory architecture in accordance with the present invention. The instant invention uses a Control Block for performing read/write and compare operations in parallel. The Control Block provides the flexibility to choose either to perform any one of the read/write/compare operations in normal mode or to perform the read/write and compare operations in combined mode.

[00015] In the normal mode compare operation the Control Block uses the Compare Data Write Driver to feed the compare data into the memory core through the bit lines. The bitline data is compared with the data stored in each cell of the Core. The results of the compare

operation are then fed to the Match Block. The Match block generates a hit signal for the highest priority matching data. The Match block also provides a match/mismatch signal to the ROM encoder/Cache.

[00016] The Control Block sends a signal to Read/Write Block during the normal mode read/write operation. The address of the memory cell is decoded by the decoder with in the Read/Write Block. In case of a read operation, the word line corresponding to decoded address is enabled to provide the data contained in the memory at the bit lines. The data at the bit lines is then sensed by a sense amplifier. The output of the sense amplifier is latched in the output latch. In the case of a write operation, decoding is performed in a similar manner. Once the word line is selected, the data present at the Data input register is written on the selected line through a Write Driver.

[00017] For the combined compare and write operation, the address decoding and comparing are performed in the first half of the clock cycle. In the second half of the clock cycle the world line corresponding to the decoded address is enabled and the Write driver then performs the write operation.

[00018] For the combined compare and read operation, the address decoding and comparing are performed in first half of the clock cycle. In the second half of the clock

cycle the world line corresponding to the decoded address is enabled, to provide the data contained in the memory at the bit lines. The data at the bit lines is then sensed by a sense amplifier. The output of sense amplifier is latched in the output latch.

[00019] Figure 4 shows a data flow diagram of the decoder used for decoding the memory addresses. The decoder block has the input Address Registers followed by Address Buffers. The address is decoded in two stages with two Pre-Decoder Blocks. The Final Decoder stage generates the complete word line address.

[00020] Figure 5 shows a data flow diagram for the normal read and write operation. For write operation the data is loaded into the Data I/P Register. The Write Driver receives the data input from the Data I/P Register and assigns the data to the respective bit lines of the CAM Core. A latch based sense amplifier and a data output latch are provided for a Read operation. The output latch preserves the last read data until the next read cycle. When there is no read/write operation, the bit lines are precharged to "high".

[00021] Figure 6 shows the timing diagram of a normal read operation. =As shown in the figure Comp_En is disabled on the positive edge of the clock cycle, , and read enable line Read_En is enabled. The decoder provides the Address of the memory to be read, and when the

complete address is available the Word Line corresponding to the decoded address is enabled thereby providing data content in the memory cell to the bit lines. The data is sensed by a sense amplifier and made available at the Data Out.

[00022] Figure 7 shows the timing diagram of a normal write operation. As shown in the figure, Comp_En is disabled at the positive edge of the clock cycle, and write enable line Write_En is enabled. The decoder provides the Address of the memory to be written, and when the complete address is available, the bit lines corresponding to the address are provided with the data, while the associated Word Line is enabled connecting the bit lines to the memory cell.

[00023] Figure 8 shows the timing diagram for a normal compare operation. As shown in the figur Comp_En is enabled at the positive edge of the clock cycle, and, the compare data signal Comp_Data is enabled providing the data at the bit lines. Depending upon Match/mis-Match a hit/miss is generated.

[00024] Figure 9 shows the timing diagram for a combined compare and read operation.. In the positive phase of the clock cycle, the compare and decoding operation are performed generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The address decoder is

also activated at the positive edge of the clock for selecting a word line for the read operation from the memory. The Address is decoded for the output of the Predecoder stage or the input of the final decoder stage. The negative clock cycle triggers the reading action enables the final decoder and selects the wordline corresponding to the address for the read operation.

[00025] Figure 10 shows the timing diagram for the combined compare and write operation. The compare and decoding operations are performed at the positive phase of clock generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The positive phase of clock also activates the address decoder for selecting a word line for the write operation from the memory. The Address is decoded upto the output of the Predecoder stage or the input of the final decoder stage. The negative edge of the clock cycle triggers the writing action enables the final decoder and selects the wordline corresponding to the address input for the write operation.

[00026] It will be apparent to those with ordinary skill in the art that the foregoing is merely illustrative intended to be exhaustive or limiting, having been presented by way of example only and that various modifications can be made within the scope of the above invention. It is intended that the present

invention encompass such changes and modifications as fall within the scope of the appended claims and those that may be added during prosecution.

[00027] Accordingly, this invention is not to be considered limited to the specific examples chosen for purposes of disclosure, but rather to cover all changes and modifications, which do not constitute departures from the permissible scope of the present invention. The invention is therefore not limited by the description contained herein or by the drawings, but only by the claims as ultimately allowed.